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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/743,731 | 12/24/2003 | Takehiko Kobayashi | 500.43356X00 | 9106 |

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| EXAMINER | |
|---|---|
| NGUYEN, LEON VIET Q | |
| ART UNIT | PAPER NUMBER |
| 2611 | |

| SHORTENED STATUTORY PERIOD OF RESPONSE | MAIL DATE | DELIVERY MODE |
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| 3 MONTHS | 03/09/2007 | PAPER |

**Please find below and/or attached an Office communication concerning this application or proceeding.**

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/743,731 | KOBAYASHI, TAKEHIKO | |
| | Examiner | Art Unit | |
| | Leon-Viet Q. Nguyen | 2611 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *23 February 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-6* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6* is/are rejected.

7)☒ Claim(s) *1* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

### *Priority*

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

### *Information Disclosure Statement*

1. The information disclosure statement filed 12/24/2003 fails to comply with 37 CFR 1.98(a)(1), which requires the following: (1) a list of all patents, publications, applications, or other information submitted for consideration by the Office; (2) U.S. patents and U.S. patent application publications listed in a section separately from citations of other documents; (3) **the application number of the application in which the information disclosure statement is being submitted on each page of the list**; (4) **a column that provides a blank space next to each document to be considered, for the examiner's initials**; and (5) **a heading that clearly indicates that the list is an information disclosure statement**. The information disclosure statement has been placed in the application file, but the information referred to therein has not been considered.

### *Claim Objections*

2. Claim 1 objected to because of the following informalities:

   a. Claim 1 reads "to receive an authogonal component". It is unknown what

an authogonal component is. For the purpose of this examination, examiner will interpret authogonal to be orthogonal.

Appropriate correction is required.

### *Claim Rejections - 35 USC § 112*

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claim 4 is recites the limitation "storing the addition...". There is insufficient antecedent basis for this limitation in the claim.

### *Claim Rejections - 35 USC § 103*

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. **Claims 1 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zak et al (US6084926**.

Re claim 1, Zak discloses a demodulator of a differential detection system for a π/4 shifted QPSK or DQPSK modulation wave in digital communication (col. 2 lines 54-56), comprising:

differential detectors (detector 20 in fig. 1, col. 3 lines 8-11);

a corrector (decoder 24 in fig. 1, col. 3 lines 36-38) connected to receive outputs of said differential detectors (the output of 20 to 24 in fig. 1) for correcting a deviated distribution of signal points on a constellation (The deviated distribution is interpreted to be an error and the decoder 24 in fig. 1 has error correction capability. Furthermore it is well known in the art that a constellation is a representation of a signal modulated by a digital modulation scheme such as PSK); and

a slicer/decoder (decoder 36 in fig. 1, col. 4 lines 50-52) connected to receive outputs of said corrector (the output of 24 to 36 in fig. 1),

wherein said slicer/decoder decodes a received bit from the signal points after the deviated distribution thereof is corrected (fig. 1, col. 4 lines 22-26, the decoder 36 receives the bit stream from the decoder 24 in fig. 1 after error correction. It would be inherent for the decoder to decode the received data).

Zak fails to teach differential detectors each connected to receive an orthogonal component of said modulation wave. However Zak teaches a multi-path demodulator. It is well known in the art that choosing multi-path modulation techniques, such as OFDM, choose orthogonal sets of carrier frequencies. The motivation would be to prevent the different paths from interfering with each other and recovering all of the information.

Re claim 5, all of the claim limitations as recited have been analyzed and addressed in the above rejections with respect to claims 1. It would be inherent to have a method of using the apparatus as claimed in claim 1.

**7. Claims 2 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zak et al (US6084926) as applied to claim 1 above, and further in view of Akahori (US20020034266).**

Re claim 2, Zak fails to teach a corrector having average calculators and subtractors connected to the output of the differential detector and subtracts an average value of the output of the differential detector from the output of the differential detector. However Akahori teaches a demodulator wherein said corrector (components 18 and 20 in fig. 1) has average calculators each connected to receive an output of respective one of the differential detectors (phase error detector 18 in fig. 1, ¶0080. The phase error detector includes a circuit to find the average) and subtractors each connected to receive an output of respective one of the differential detectors (phase corrector 20 in fig. 1, ¶0082. The phase corrector subtracts the phase difference information from the phase deviation information) and also receive an associated one of outputs of the average calculators for subtracting an average value of the output of the differential detector from the output of the differential detector (¶0048, ¶0080, ¶0082. The phase corrector 20 in fig. 1 subtracts the phase difference information, which is output of phase error detector 20 in fig. 1, from the received phase deviation information. The phase deviation information is the output of differential circuit 54 in fig. 1, which is part of the differential detector 56 in fig. 1).

Therefore taking the combined teachings of Zak and Akahori as a whole, it would have been obvious to one of ordinary skill in the art at the time the invention was made

to incorporate the corrector of Akahori into the demodulator of Zak. The motivation to combine Akahori and Zak would be to more efficiently find an average when the input signal includes noises (¶0080) and remove a carrier frequency phase error (¶0082).

Re claim 6, Zak teaches a method wherein a slicer/decoder decodes a received bit from said signal points of said modulation wave after an average value is subtracted (speech decoder 36 in fig. 1 performs decoding after correcting is done in decoder 24).

However Zak fails to teach the correcting step including the steps of calculating an average value of the signal points of said differential-detected modulation wave; and subtracting said average value from each of the signal points of said differential-detected modulation wave. Akahori does teach calculating an average value of the signal points of said differential-detected modulation wave (¶0080); and subtracting said average value from each of the signal points of said differential-detected modulation wave (¶0048, ¶0080, ¶0082. The phase corrector 20 in fig. 1 subtracts the phase difference information, which is output of phase error detector 20 in fig. 1, from the received phase deviation information. The phase deviation information is the output of differential circuit 54 in fig. 1, which is part of the differential detector 56 in fig. 1).

Therefore taking the combined teachings of Zak and Akahori as a whole, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the corrector of Akahori into the demodulator of Zak. The motivation to combine Akahori and Zak would be to more efficiently find an average when the input signal includes noises (¶0080) and remove a carrier frequency phase error (¶0082).

**8. Claims 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Zak et al (US6084926) and Akahori (US20020034266) as applied to claim 1 above, in view of Lim (US5588027) and further in view of Sano et al (US6836518).**

Re claim 3, the modified invention of Zak and Akahori teaches a demodulator wherein said average calculators each include an adder for adding together said N pieces of output data read out from the memory (¶0080. Although not explicitly taught, it would be obvious and necessary to have an adder which adds up the four detected values), N being an integer of 2 or more (¶0080, N being four). The modified invention of Zak and Akahori fails a memory for storing N pieces of output data of said differential detector. However Lim teaches an intermediate buffer memory which stores data from a first and second A/D converter (col. 3 lines 9-11).

Therefore taking the modified invention of Zak and Akahori and the teaching of Lim as a whole, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the memory buffer of Lim into the demodulator of Zak and Akahori. The motivation to combine Sano, Zak, and Akahori for synchronization because the write speed from the A/D converters differs from the read speed of a digital processing circuit (col. 3 lines 9-12).

The modified invention of Zak and Akahori also fails to teach a multiplier for outputting an output corresponding to 1/N of its input. However Sano teaches a multiplier, which multiplies a correlation value input by 1/N (col. 11 lines 22-26).

Therefore taking the modified invention of Zak and Akahori and the teaching of Sano as a whole, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the multiplier of Sano into the demodulator of Zak and Akahori. The motivation to combine Sano, Zak, and Akahori would be to avoid synchronization of the receiver with a reflected wave (col. 11 lines 27-28).

**9. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Zak et al (US6084926) and Akahori (US20020034266) as applied to claim 1 above, in view of Sano et al (US6836518) and further in view of Betts et al (US4796279).**

Re claim 4, the modified invention of Zak and Akahori teaches an output of said adder is an average value of the output data of the differential detector (Akahori: phase error detector 18 in fig. 1, ¶0080. The phase error detector includes a circuit to find the average and it would be necessary to have an adder to add up the four detected values) and an adder for adding together outputs (¶0080) but fails to teach average calculators including a first multiplier for multiplying output data by a constant, a second multiplier for multiplying data from the register by a constant α, wherein and the constant α is set to satisfy a relationship $0 < \alpha < 1$.

However Sano teaches a first multiplier (multiplier 8 in fig. 9) for multiplying output data by a constant (fig. 9, although not explicitly shown it would be obvious to multiply the input from 7 to multiplier 8 by some predetermined value since there are no other inputs), a second multiplier (multiplier 33 in fig. 9) for multiplying data from the

register by a constant α (col. 11 lines 22-26, 1/N is interpreted to be the same as the constant α), and an adder for adding together outputs of said first and second multipliers (comparator 17 in fig. 9, it is well known in the art that comparators can be used as adders), wherein and the constant α is set to satisfy a relationship $0 < \alpha < 1$ (col. 11 lines 22-26, col. 12 lines 37-39).

Therefore taking the modified invention of Zak and Akahori and the teaching of Sano as a whole, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the multiplier of Sano into the demodulator of Zak and Akahori. The motivation to combine Sano, Zak, and Akahori would be to avoid synchronization of the receiver with a reflected wave (col. 11 lines 27-28).

The modified invention of Zak and Akahori also fails to teach average calculators including a register and storing the addition in said register. However Betts teaches a register (register 74 in fig. 4) for storing the sum of two multipliers (multipliers 48 and 50 summed in adder 52 in fig. 4).

Therefore taking the modified invention of Zak and Akahori and the teaching of Betts as a whole, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate register of Betts into the demodulator of Zak and Akahori. The motivation to combine Betts, Zak, and Akahori would be to store decoded data from a remote modem (col. 2 line 67 - col. 3 line 4)

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Leon-Viet Q. Nguyen whose telephone number is 571-270-1185. The examiner can normally be reached on monday-friday, alternate friday off, 7:30AM-5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David C. Payne can be reached on 571-272-3024. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Leon-Viet Nguyen/